Claims

What is claimed is:

1. An autonomous error recovery method for a memory device of a computing system, said method comprising:

testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor; and

automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment responsive to the request, wherein the memory device and the second memory device comprise separate memory devices.

2. The method of claim 1, wherein the testing and the automatically retrieving are transparent to a requester making the request for the addressed data.

3. The method of claim 1, wherein the memory device comprises a cache, and the second memory device comprises a main memory of the computing system.

4. The method of claim 1, wherein the automatically retrieving further comprises processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

5. The method of claim 1, wherein the testing further comprises parity checking the associated control information.

6. The method of claim 1, wherein the testing further comprises detecting an uncorrectable error in a code word corresponding to the addressed data, wherein the code word was generated by applying an error detecting code to data sent to the memory device for storage.

7. An autonomous error recovery method for a memory device of a computing system, said method comprising:

testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor;

ascertaining from a change bit of the associated control information whether the addressed data has changed since contents of an addressed storage compartment of a second memory device were written to the memory device as the addressed data, wherein the memory device and the second memory device comprise separate memory devices; and

automatically retrieving the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, and providing the contents of the addressed storage compartment responsive to the request, otherwise denying access to the addressed data and to the contents of the addressed storage compartment of the second memory device responsive to the request if error is detected by the testing and the addressed data has changed.

8. The method of claim 7, wherein the automatically retrieving further comprises replacing corrupted addressed data in the memory device with the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, as determined by the ascertaining.

9. The method of claim 7, wherein:

the contents of the addressed storage compartment of the second memory device comprise back-up data and control information associated with the back-up data; and

the providing further comprises

determining whether the back-up data or the control information associated with the back-up data contains an uncorrectable error; and

refusing access to the contents of the addressed storage compartment of the second memory device responsive to the request if the determining detects an uncorrectable error.

10. The method of claim 7, wherein the automatically retrieving further comprises processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

11. The method of claim 7, wherein

the testing, ascertaining, and the automatically retrieving are transparent to a requester making the request;

the memory device comprises a cache; and

the second memory device comprises a main memory of the computing system.

12. An autonomous error recovery system for a memory device of a computing system, said system comprising:

means for testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor; and

means for automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment responsive to the request, wherein the memory device and the second memory device comprise separate memory devices.

13. The system of claim 12, wherein the means for testing and the means for automatically retrieving are transparent to a requester making the request for the addressed data.

14. The system of claim 12, wherein the memory device comprises a cache, and the second memory device comprises a main memory of the computing system.

15. The system of claim 12, wherein the means for automatically retrieving further comprises means for processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

16. The system of claim 12, wherein the means for testing further comprises means for parity checking the associated control information.

17. The system of claim 12, wherein the means for testing further comprises means for detecting an uncorrectable error in a code word corresponding to the addressed data, wherein the code word was generated by applying an error detecting code to data sent to the memory device for storage.

18. An autonomous error recovery system for a memory device of a computing system, said system comprising:

means for testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor;

means for ascertaining from a change bit of the associated control information whether the addressed data has changed since contents of an addressed storage compartment of a second memory device were written to the memory device as the addressed data, wherein the memory device and the second memory device comprise separate memory devices; and

means for automatically retrieving the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, and for providing the contents of the addressed storage compartment responsive to the request, otherwise denying access to the addressed data and to the contents of the addressed storage compartment of the second memory device responsive to the request if error is detected by the testing and the addressed data has changed.

19. The system of claim 18, wherein the means for automatically retrieving further comprises means for replacing corrupted addressed data in the memory device with the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, as determined by the means for ascertaining.

20. The system of claim 18, wherein:

the contents of the addressed storage compartment of the second memory device comprise back-up data and control information associated with the back-up data; and

the means for providing further comprises

means for determining whether the back-up data or the control information associated with the back-up data contains an uncorrectable error; and

means for refusing access to the contents of the addressed storage compartment of the second memory device responsive to the request if the means for determining detects an uncorrectable error.

21. The system of claim 18, wherein the means for automatically retrieving further comprises means for processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

22. The system of claim 18, wherein

the means for testing, the means for ascertaining, and the means for automatically retrieving are transparent to a requester making the request;

the memory device comprises a cache; and

the second memory device comprises a main memory of the computing system.

23. A cache with autonomous error recovery for a computing system, said cache comprising:

logic adapted to test addressed data and associated control information of a cache memory for error, wherein the addressed data is to be provided responsive to a request therefor; and

wherein the logic is further adapted to automatically retrieve contents of an addressed storage compartment of a second memory device if error is detected, and to provide the contents of the addressed storage compartment responsive to the request, wherein the cache and the second memory device comprise separate memory devices.

24. A cache with autonomous error recovery for a computing system, said cache comprising:

logic adapted to test addressed data and associated control information of a cache memory for error, wherein the addressed data is to be provided responsive to a request therefor;

wherein the logic is further adapted to ascertain from a change bit of the associated control information whether the addressed data has changed since contents of an addressed storage compartment of a second memory device were written to the memory device as the addressed data, wherein the cache and the second memory device comprise separate memory devices; and

wherein the logic is also adapted to automatically retrieve the contents of the addressed storage compartment of the second memory device if error is detected and the addressed data has not changed, and provide the contents of the addressed storage compartment responsive to the request, otherwise to deny access to the addressed data and to the contents of the addressed storage compartment of the second memory device responsive to the request if error is detected and the addressed data has changed.

25. At least one program storage device readable by a machine embodying at least one program of instructions executable by the machine to perform an autonomous error recovery method for a memory device of a computing system, said method comprising:

testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor; and

automatically retrieving contents of an addressed storage compartment of a second memory device if error is detected by the testing, and providing the contents of the addressed storage compartment responsive to the request, wherein the memory device and the second memory device comprise separate memory devices.

26. The at least one program storage device of claim 25, wherein the testing and the automatically retrieving are transparent to a requester making the request for the addressed data.

27. The at least one program storage device of claim 25, wherein the memory device comprises a cache, and the second memory device comprises a main memory of the computing system.

28. The at least one program storage device of claim 25, wherein the automatically retrieving further comprises processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

29. The at least one program storage device of claim 25, wherein the testing further comprises parity checking the associated control information.

30. The at least one program storage device of claim 25, wherein the testing further comprises detecting an uncorrectable error in a code word corresponding to the addressed data, wherein the code word was generated by applying an error detecting code to data sent to the memory device for storage.

31. At least one program storage device readable by a machine embodying at least one program of instructions executable by the machine to perform an autonomous error recovery method for a memory device of a computing system, said method comprising:

testing addressed data and associated control information of a memory device for error, wherein the addressed data is to be provided responsive to a request therefor;

ascertaining from a change bit of the associated control information whether the addressed data has changed since contents of an addressed storage compartment of a second memory device were written to the memory device as the addressed data, wherein the memory device and the second memory device comprise separate memory devices; and

automatically retrieving the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, and providing the contents of the addressed storage compartment responsive to the request, and otherwise denying access to the addressed data and to the contents of the addressed storage compartment of the second memory device responsive to the request if error is detected by the testing and the addressed data has changed.

32. The at least one program storage device of claim 31, wherein the automatically retrieving further comprises replacing corrupted addressed data in the memory device with the contents of the addressed storage compartment of the second memory device if error is detected by the testing and the addressed data has not changed, as determined by the ascertaining.

33. The at least one program storage device of claim 31, wherein:

the contents of the addressed storage compartment of the second memory device comprise back-up data and control information associated with the back-up data; and

the providing further comprises

determining whether the back-up data or the control information associated with the back-up data contains an uncorrectable error; and

refusing access to the contents of the addressed storage compartment of the second memory device responsive to the request if the determining detects an uncorrectable error.

34. The at least one program storage device of claim 31, wherein the automatically retrieving further comprises processing the request as if the addressed data were missing from the memory device if an error is detected by the testing.

35. The at least one program storage device of claim 31, wherein

the testing, ascertaining, and the automatically retrieving are transparent to a requester making the request;

the memory device comprises a cache; and

the second memory device comprises a main memory of the computing system.

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